	U	1 [1]	Document ID	Issue Date	Pages	Title	Current OR
1	☐	☒	US 6143663 A	20001107	16	Employing deionized water and an abrasive surface to polish a semiconductor topography	438/691
2	☐	☒	US 6114215 A	20000905	10	Generating non-planar topology on the surface of planar and near-planar substrates	438/401
3	☐	☒	US 5922620 A	19990713	12	Chemical-mechanical polishing (CMP) method for controlling polishing rate using ionized water, and CMP apparatus	438/693
4	☐	☒	US 5602423 A	19970211	10	Damascene conductors with embedded pillars	257/752

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5	Image Doc. Displayed	PT
1	257/E21.245; 257/E21.304; 438/692; 438/693		Koutny, Jr., William W. C.	☒	☐	☐	☐	☐	☐	☐	US 6143663	☐
2	257/E23.179; 438/633; 438/692; 438/693		Osugi, Richard S. et al.	☒	☐	☐	☐	☐	☐	☐	US 6114215	☐
3	257/E21.23; 257/E21.304; 438/4; 438/690; 438/692; 451/60		Shimomura, Mariko et al.	☒	☐	☐	☐	☐	☐	☐	US 5922620	☐
4	257/760; 257/763; 257/764; 257/765; 257/767; 257/768; 257/E21.575		Jain, Manoj K.	☒	☐	☐	☐	☐	☐	☐	US 5602423	☐

L Number	Hits	Search Text	DB	Time stamp
1	1	("6232231").PN.	USPAT; US-PGPUB	2003/05/02 14:04
2	3	(("5721172") or ("5943590") or ("5928959")).PN.	USPAT; US-PGPUB	2003/05/02 14:24
3	7	trench same CMP same deionized	USPAT; US-PGPUB	2003/05/02 14:27
4	0	trench same CMP same deionized	EPO; JPO; DERWENT; IBM_TDB	2003/05/02 14:27
5	1	trench and (CMP same deionized)	EPO; JPO; DERWENT; IBM_TDB	2003/05/02 14:28
6	92	trench and (CMP same deionized)	USPAT; US-PGPUB	2003/05/02 14:43
7	2385	438/691,692,697,700.ccls.	USPAT; US-PGPUB	2003/05/02 14:41
8	634	438/691,692,697,700.ccls. and trench and cmp	USPAT; US-PGPUB	2003/05/02 14:52
12	84	(438/691,692,697,700.ccls. and trench and cmp) and (deionized)	USPAT; US-PGPUB	2003/05/02 14:52

US-PAT-NO: 6114215

DOCUMENT-IDENTIFIER: US 6114215 A

TITLE: Generating non-planar topology on the surface of planar and near-planar substrates

---------- KWIC ---------

FIGS. 2A-2C show some major steps involved in the fabrication of one of alignment marks 16 on a surface of an IC substrate 20. The fabrication of alignment mark 16 may begin when a **trench** 24 is etched in a dielectric layer 22, as shown in FIG. 2A. According to FIG. 2B, a layer of metal 26 is then deposited on the surface of IC substrate 20, filling **trench** 24. Next, the surface of IC substrate 20 is subjected to chemical-mechanical polishing for polishing layer of metal 26 disposed above dielectric layer 22 and form alignment mark 16 as shown in FIG. 2C. Chemical-mechanical polishing (sometimes referred to as "CMP") typically involves mounting IC substrates face down on a substrate holder and rotating the IC substrate against a polishing pad mounted on a platen, which is in turn rotating or is in orbital state. A slurry containing a chemical that chemically interacts with the facing IC substrate layer and an abrasive that physically removes that layer is flowed between the IC substrate and the polishing pad or on the pad near the IC substrate. In semiconductor wafer fabrication, this technique is used to planarize various wafer layers such as dielectric layers, metallization layers etc.

The step of fabricating the alignment mark may include: (i) etching a **trench** in a surface of a dielectric layer that is disposed above the integrated circuit substrate surface; (ii) blanket depositing the alignment mark fill material on the surface of the dielectric layer and filling the **trench**; and (iii) polishing the integrated circuit substrate surface to remove the alignment mark fill material deposited above the surface of the dielectric layer and excessive amounts of the alignment mark fill material deposited above the **trench** and thereby form the alignment mark.

The dielectric layer may be silicon dioxide. The **trench** may have a width that is between about 0.5 and about 8 .mu.m and a length that is between about 80 and about 120 .mu.m. The depth of the **trench** may depend on the thickness of the dielectric layer, for example, and is generally between about 3000 Angstroms and about 2 .mu.m. The alignment mark fill material may include a metal, e.g., tungsten.

FIG. 3A shows a partially fabricated integrated circuit (IC) substrate, e.g., a partially fabricated semiconductor wafer, 100 having a modified alignment mark 116, according to one embodiment of the present invention, that is formed in a dielectric layer 122. Alignment mark 116 includes a **trench** 124 partially filled with an alignment mark fill material 126, which is similar to a plug composition, i.e. a contact or via plug composition, and therefore may include a metal like tungsten, for example. **Trench** 124 may have a width that is between about 0.5 and about 8 .mu.m and a length that is between about 80 and about 120 .mu.m. A depth of **trench** 124 may depend on the application and

thickness of dielectric layer 122 and is generally between about 3000 Angstroms
and about 2 .mu.m.

In an another embodiment, step 204 of the present invention is performed
during fine polishing of the partially fabricated IC substrate surface.
Typically during fine polishing, also well known in the art as "buffing," an IC
substrate surface undergoes polishing that is far less coarse than the **CMP**
process described in step 202. Fine polishing is typically carried out in the
presence of a buffing solution, which generally does not contain abrasive
particles to initiate any abrasions on the IC substrate surface during fine
polishing. This step is typically employed in some IC substrate fabrication
applications to remove a contaminated IC substrate layer, i.e. including
contaminants from the slurry residue and/or eroded material, resulting from the
CMP process. Conventionally, the buffing solution includes a dilute solution
of a surfactant, such as between about 1% and about 3% (in volume) of ammonium
hydroxide (NH.sub.4 OH) in **deionized** water. According to one embodiment of the
present invention, however, the metal etchant described above is admixed with
the buffing solution. Consequently, at least some of the alignment mark fill
material is selectively removed from the IC substrate surface during the fine
polishing of the IC substrate surface and a step is introduced into the
alignment mark as shown in FIG. 3A.

In yet another embodiment, step 204 of the present invention is performed in
a wet storage station that typically follows **CMP** or fine polishing. Typically,
the IC substrates are soaked or drenched in a bath of **deionized** water, before
they are subjected to vigorous cleaning in a wafer scrubber

by various cleaning
solutions. In this embodiment, the metal etchant mentioned above is admixed
with the soaking solution, e.g., including **deionized** water, employed in the wet
storage station to selectively remove the alignment mark fill material from IC
substrate surface and thereby introduce a step into the alignment mark.

etching a **trench** in a surface of a dielectric layer that is disposed above
said integrated circuit substrate surface;

blanket depositing said alignment mark fill material on said surface of said
dielectric layer and filling said **trench**; and

polishing said integrated circuit substrate surface to remove said alignment
mark fill material deposited above said surface of said dielectric layer and
excessive amounts of said alignment mark fill material deposited above said
trench and thereby form said alignment mark.

4. The process of claim 2, wherein said **trench** has a width that is between
about 0.5 and about 8 .mu.m.

5. The process of claim 2, wherein said **trench** has a length that is between
about 80 and about 120 .mu.m.

6. The process of claim 2, wherein said **trench** has a depth that is between
about 3000 Angstroms and about 2 .mu.m.

US-PAT-NO: 5922620

DOCUMENT-IDENTIFIER: US 5922620 A

TITLE: Chemical-mechanical polishing (CMP) method for controlling polishing rate using ionized water, and CMP apparatus

---------- KWIC ---------

FIGS. 3A and 3B show an application of the CMP method used in a process for separating **trench** elements. After an SiO.sub.2 film 2 is formed by thermal oxidation of the surface of the semiconductor substrate 1, an Si.sub.3 N.sub.4 film 7 which will serve as a stopper film is formed by the CVD method. Subsequently, the films 2 and 7 are patterned by lithography to form grooves 9. Those surface portions of the semiconductor substrate 1 which constitute the inner surfaces of the grooves 9 are oxidized, and then boron is injected into the bottoms of the grooves 9 to form channel cut regions 10. Thereafter, a polysilicon film 3 is formed by the CVD method on the Si.sub.3 N.sub.4 film 7 and in the grooves 9 (FIG. 3A). An SiO.sub.2 film may be used in place of the polysilicon film. Then, the polysilicon film 3 on the semiconductor substrate 1 is polished until the Si.sub.3 N.sub.4 film 7 is exposed (FIG. 3B). In this case, a polishing rate as low as about 1/10-1/200 is employed, and hence the polishing can be stopped when the Si.sub.3 N.sub.4 film 7 is exposed. Thus, the polysilicon film 3 is formed only in the grooves 9. As is evident from the above, the polishing can be stopped just when the stopper

film is exposed, by using, as the stopper film, a film of a polishing rate lower than that of a film to be polished, and designating an appropriate polishing period of time.

2. The **CMP** method according to claim 1, wherein the ionized water is created by electrolyzing **deionized** water.

11. The **CMP** method according to claim 10, wherein the ionized water is created by electrolyzing **deionized** water.

Miyashita et al., "A New Post CMP Cleaning Method for **Trench** Isolation Process," First International Chemical-Mechanical Polish (C.M.P.) for VLSI/ULSI Multilevel Interconnection Conference (CMP-MIC), pp. 159-168, 1996.

US-PAT-NO: 5602423

DOCUMENT-IDENTIFIER: US 5602423 A

TITLE: Damascene conductors with embedded pillars

---------- KWIC ---------

An improved damascene process is claimed by Cote et al. in U.S. Pat. No. 5,262,354, issued on Nov. 16, 1993. Cote et al. cite several problems with damascene polishing used directly on low resistivity, soft metals such as Al-Cu alloys, including scratching, smearing, corrosion, and dishing (conducting material may be removed to a level below the top surface of the insulator). Their approach to this problem involves depositing the soft metal such that the channels are filled to between a few hundred nm and a few hundred .ANG. of the top surface of the dielectric, and capping this with a wear-resistant, higher resistivity layer (e.g. a refractory metal such as tungsten) before polishing. One difficulty with such an approach is the exacting control required for an anisotropic deposition of the soft metal to the required depth tolerance, particularly given normal variations in **trench** depth and metal deposition rate across a wafer. The higher resistivity refractory cap layer also results in an increase in resistance for all conductors fabricated on a given level, unless compensations in conductor height and/or width are incorporated in the design.

During damascene polishing, polish conditions are generally selected which provide a much faster relative polish rate for the

conductive film, as compared to the polish rate of the underlying insulating layer. The present invention therefore realizes that pillars of an appropriate height may be dispersed within a large channel as wear-resistant polish pad supports, before deposition of a conducting film. The pillars serve structurally to prevent overetching or dishing in such a large channel by acting as an etch stop for polishing of the conducting material deposited over a wide **trench**. One method of forming such pillars is to make provision for them on the mask used to pattern the channels, such that a pillar of the underlying insulating layer material remains after the channel is formed. Alternately, a separate layer of either insulating or conducting material (harder to polish than a subsequent conducting film) may be deposited and patterned to form a pillar within a channel.

FIG. 2B shows a wide inlaid conductor 30 and a narrow inlaid conductor 32 remaining in channels 24 and 26, respectively, after polishing to remove unneeded sections of film 28. Polishing is preferably accomplished by chemical-mechanical polishing (**CMP**), wherein a wafer containing substrate 20 and/or a polishing pad are rotatably mounted and brought into contact with each other under rotation. A slurry providing both abrasive and chemically reactive components is supplied, typically to the pad, during polishing. The abrasive component is typically comprised of finely ground colloidal silica or alumina particles. For metal polishing, the chemically reactive component is typically diluted acid and/or hydrogen peroxide, with the remainder of the slurry comprised of **deionized** water. In general, it is desirable that the slurry composition and polishing conditions (e.g. rotational velocity, polish force,

temperature) be adjusted such that the conducting film is selectively removed
at a faster rate than the insulating layer (30:1 being a typical ratio) during
CMP. One drawback of such a process, however, is illustrated in FIG. 2B. The
top surface of narrow conductor 32 is shown as slightly dished but
substantially coplanar with the upper surface of insulating layer 22. Wide
conductor 30, shown here as 3 times the width of the small conductor (some
conductors may be much wider on a given circuit), is shown as both recessed
(i.e. overetched) and severely dished. In extreme cases, sections of a wide
conductor may be completely removed from the channel during polishing.

US-PAT-NO: 6027554

DOCUMENT-IDENTIFIER: US 6027554 A

TITLE: Polishing composition

---------- KWIC ---------

On the other hand, a study is being made to apply the CMP technique to planarization of an interlayer dielectric such as a silicon dioxide film, a wiring material such as an aluminum, tungsten or copper film, or a polysilicon film, to separation of elements and to other applications. A shallow **trench** isolation method may be mentioned as one of methods for isolation of elements, which have been studied in recent years. This method comprises forming a shallow **trench** in silicon, forming a silicon dioxide film thereon, followed by planarization by the CMP technique, whereby isolation of elements can be made in a narrower area, and it has attracted an attention as a technique useful for densification of semiconductor devices.

Technical objectives in carrying out the shallow **trench** isolation are to uniformly finish without excessive or insufficient stock removal by polishing the surface for planarization and to complete the polishing at a predetermined level of stock removal. Usually, it is common to provide a harder silicon nitride film beneath a silicon dioxide film to be polished, so that the silicon nitride film serves as a stopper during the polishing. It should readily be understood that as a polishing agent to be used here, it is preferred to employ a polishing agent which is capable of efficiently polishing the silicon dioxide film and which, on the other hand, is incapable of polishing the silicon nitride film.

The water to be used in the present invention is not particularly limited, and it may, for example, be industrial water, city water, **deionized** water, distilled water or ultrapure water. The content of the water in the polishing composition is usually from 30 to 99.899 wt %, preferably from 65 to 98.995 wt %.

438/692

US-PAT-NO: 5922620

DOCUMENT-IDENTIFIER: US 5922620 A

TITLE: Chemical-mechanical polishing (CMP) method for controlling polishing rate using ionized water, and CMP apparatus

---------- KWIC ---------

FIG. 1 is a schematic sectional view, showing a general CMP apparatus for flattening a wafer surface. As is shown in FIG. 1, a turn table 16, which includes a polishing disc 17 and a support unit 15, is placed on a stage 11 with a bearing 13 interposed therebetween. A polishing pad 19 is attached to the upper surface of the polishing disc 17 for polishing a wafer. A driving shaft 21 is provided for rotating the turn table 16. The driving shaft 21 is rotated by a motor 23 via a rotating belt 25. On the other hand, a semiconductor wafer 20 is supported by a wafer carrier 33. The wafer carrier 33 has a retainer ring 29 and an adsorption pad 31 for holding the wafer by a vacuum force or the tension of water. The wafer 20 has its position controlled by the wafer carrier 33 such that it is opposed to the polishing pad 19. The wafer carrier 33 is connected to a driving shaft 35. The driving shaft 35 is rotated by a motor 37 via gears 39 and 40, and **fixed** to a driving unit 43 for vertically move the shaft 35.

FIGS. 3A and 3B show an application of the CMP method used in a process for separating **trench** elements. After an SiO.sub.2 film 2 is formed by thermal oxidation of the surface of the semiconductor substrate 1, an Si.sub.3 N.sub.4 film 7 which will serve as a stopper film is formed by the CVD method. Subsequently, the films 2 and 7 are patterned by lithography to form grooves 9.

Those surface portions of the semiconductor substrate 1 which constitute the inner surfaces of the grooves 9 are oxidized, and then boron is injected into the bottoms of the grooves 9 to form channel cut regions 10. Thereafter, a polysilicon film 3 is formed by the CVD method on the Si.sub.3 N.sub.4 film 7 and in the grooves 9 (FIG. 3A). An SiO.sub.2 film may be used in place of the polysilicon film. Then, the polysilicon film 3 on the semiconductor substrate 1 is polished until the Si.sub.3 N.sub.4 film 7 is exposed (FIG. 3B). In this case, a polishing rate as low as about 1/10-1/200 is employed, and hence the polishing can be stopped when the Si.sub.3 N.sub.4 film 7 is exposed. Thus, the polysilicon film 3 is formed only in the grooves 9. As is evident from the above, the polishing can be stopped just when the stopper film is exposed, by using, as the stopper film, a film of a polishing rate lower than that of a film to be polished, and designating an appropriate polishing period of time.

It is not considered preferable these days to use a fluorine-based solvent such as fleon, etc. in manufacturing semiconductor devices, since it adversely affects the environment. In place of the fluorine-based solvent, **deionized** water has recently been used as the safest solvent. **Deionized** water is of high purity with a resistance of about 5 to 18 M.OMEGA.cm, which contains almost no impurities including ions, fine particles, microbes, organic matters, etc. A water purifying apparatus (deionizer) very efficiently removes materials suspended or dissolved in water, thereby creating extremely pure water. **Deionized** water may also be called "pure water" when its electric conductivity .rho. is lower than 10 .mu.Scm, and "extrapure water" when it is lower than 0.055 .mu.Scm.

In the present invention, **deionized** water is electrolyzed to create highly-oxidizable positive-ionized water which contains oxygen and ozone, and highly-reducible negative-ionized water. These positive-ionized water and negative-ionized water are used for chemical-mechanical polishing.

Ionized water supplied from the ionized-water supply pipe 52 can be classified into alkaline ionized water and acidic ionized water. Ionized water of a desired pH is created by electrolyzing, at a low voltage, **deionized** water

which contains no electrolyte, i.e. no metal impurity, in an electrolytic bath with a solid electrolyte contained therein. Where alkaline ionized water is used and the polishing rate is changed during polishing, the rate can be increased in a stable manner by increasing the pH value of alkaline ionized water, and can be reduced in a stable manner by reducing the pH value of alkaline ionized water. On the other hand, in the case of using acidic ionized water, the polishing rate can be increased in a stable manner by reducing the pH value of acidic ionized water, and can be reduced in a stable manner by increasing the pH value of acidic ionized water.

In the electrolytic bath 60, a diluent electrolyte solution 69 with a supporting electrolyte (e.g. ammonium chloride) contained therein is mixed with **deionized** water, and a power voltage is applied thereto from the battery 66, thereby electrolyzing the **deionized** water. Negative-ionized water 73 created on the side of the cathode 63 as a result of electrolyzation is alkaline ionized water, while positive-ionized water 74 created on the side of the anode 64 is acidic ionized water. Moreover, if **deionized** water is electrolyzed in the bath 60 using oxalic acid as the supporting electrolyte, both negative-ionized water created on the side of the cathode and positive-ionized water created on the side of the anode exhibit acidic properties. The negative-ionized water 73 in the cathode chamber 61 is supplied to the outside through a negative-ionized water supply pipe 71, and the positive-ionized water in the anode chamber 62 is supplied to the outside through a positive-ionized water supply pipe 72.

Ionized water can be classified into alkaline ionized water and acidic ionized water. Ionized water of a desired pH is created by electrolyzing, at a low voltage, **deionized** water which contains no electrolyte, i.e. no metal impurity, in an electrolytic bath with a solid electrolyte contained therein. Where in the case of using alkaline ionized water, the polishing rate is changed during polishing, it can be increased in a stable manner by increasing the pH value of alkaline ionized water, and can be reduced in a stable manner by reducing the pH value of alkaline ionized water. On the other hand, in the case of using acidic ionized water, the polishing rate can be increased in a

stable manner by reducing the pH value of acidic ionized water, and can be reduced in a stable manner by increasing the pH value of acidic ionized water.

2. The CMP method according to claim 1, wherein the ionized water is created by electrolyzing **deionized** water.

11. The CMP method according to claim 10, wherein the ionized water is created by electrolyzing **deionized** water.

438/692

Miyashita et al., "A New Post CMP Cleaning Method for **Trench** Isolation Process," First International Chemical-Mechanical Polish (C.M.P.) for VLSI/ULSI Multilevel Interconnection Conference (CMP-MIC), pp. 159-168, 1996.